UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/823,859	04/14/2004	Hee-Cheol Choi	SAM-0522	6192

7590 11/15/2007

Steven M. Mills
MILLS & ONELLO LLP
Suite 605
Eleven Beacon Street
Boston, MA 02108

EXAMINER	
MISLEH, JUSTIN P	

ART UNIT	PAPER NUMBER
2622	

MAIL DATE	DELIVERY MODE
11/15/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/823,859	CHOI, HEE-CHEOL	
	Examiner	Art Unit	
	Justin P. Misleh	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 August 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 50* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 August 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed August 24, 2007 have been fully considered but they are not persuasive.

2. Applicant argues, "Johnson, et al. fails to teach or suggest an image processing system [and corresponding method] that includes a CDS which includes a variable capacitance unit having first and second variable input capacitances ... [instead], in Johnson, et al., the first stage includes only a single variable capacitor 135."

The Examiner respectfully disagrees with Applicant's position. Johnson et al. disclose a correlated double sampler (CDSVGA 114) for receiving the input signal (VIN), sampling the input signal (see paragraph 0068) and providing an output signal (output signal provided to ADC 116 – see figure 3), the CDS (CDSVGA 114) comprising an amplifier for amplifying the input signal (see figure 5) and a variable capacitance unit (see figure 5) having first (C2) and second (C3) variable input capacitances (see paragraph 0068).

As clearly shown in figure 5, the CDSVGA (114) has two-stages (131 and 132, respectively) each with a variable input capacitance (C2 and C3, respectively).

Therefore, the Examiner maintains the rejection.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. **Claims 1, 2, 4 – 16, 18 – 27, 29 – 41, and 43 – 50** are rejected under 35 U.S.C. 102(b) as being anticipated by Johnson et al. (US 2002/0176009).

Claims 1, 2, 4 – 16, and 18 – 25 and **Claims 26, 27, 29 – 41, and 43 – 50** appear to be corresponding apparatus and method claims, respectively, that are substantively identical in scope. For sake of brevity, they will be rejected together.

5. For **Claims 1 and 26**, Johnson et al. disclose an image processing system (analog image processing system 113 – see figure 3), comprising:

an input for receiving an input signal (VIN – see figures 3 and 5); and

a correlated double sampler (CDSVGA 114) for receiving the input signal (VIN), sampling the input signal (see paragraph 0068) and providing an output signal (output signal provided to ADC 116 – see figure 3), the CDS (CDSVGA 114) comprising an amplifier for amplifying the input signal (see figure 5) and a variable capacitance unit (see figure 5) having first (C2) and second (C3) variable input capacitances (see paragraph 0068).

6. For **Claims 15 and 40**, Johnson et al. disclose an image processing system (analog image processing system 113 – see figure 3), comprising:

a correlated double sampler (CDSVGA 114) for receiving the input signal (VIN), sampling the input signal (see paragraph 0068) and providing an output signal (output signal provided to ADC 116 – see figure 3), the CDS (CDSVGA 114) comprising an amplifier for amplifying the input signal (see figure 5) and a variable capacitance unit (see figure 5) having first (C2) and second (C3) variable input capacitances (see paragraph 0068); and

a programmable gain amplifier (digital gain 117; see figure 8) for receiving the output signal from the CDS (CDSVGA 114) and amplifying the received signal (see figure 3, the output of the CDSVAGA 114 is passed through ADC 116 and on to digital gain 117).

7. As for **Claims 2, 16, 27, and 41**, Johnson et al. disclose wherein gain in the CDS is settable to one of a plurality of levels (see paragraphs 0067 and 0068).

8. As for **Claims 4, 18, 29, and 43** Johnson et al. disclose wherein gain in the CDS is settable to a level between 1.0 and 2.0 (see paragraph 0067, lines 22 – 26).

9. As for **Claims 5 and 30**, Johnson et al. disclose wherein gain in the CDS is settable by a digital input signal (see paragraph 0067, lines 20 – 22, "8 bit control word").

10. As for **Claims 6 and 31**, Johnson et al. disclose wherein the digital input signal contains a plurality of bits (see paragraph 0067, lines 20 – 22, "8 bit control word").

11. As for **Claims 7 and 32**, Johnson et al. disclose, as shown in figure 8, a programmable gain amplifier (digital gain 117) for receiving the output signal from the CDS (CDSVGA 114) and amplifying the received signal (see figure 3, the output of the CDSVAGA 114 is passed through ADC 116 and on to digital gain 117).

12. As for **Claims 8, 19, 33, and 44**, Johnson et al. disclose, as shown in figures 8 and 9, wherein gain in the PGA is settable to one of a plurality of levels (see paragraphs 0071 and 0072).

13. As for **Claims 9, 20, 34, and 45**, Johnson et al. disclose wherein gain in the PGA is settable to a level between 1.0 and 2.0 (see paragraph 0067, lines 22 – 26).

14. As for **Claims 10 and 35**, Johnson et al. disclose wherein gain of the PGA is settable by a digital input signal (see paragraph 0067, lines 20 – 22, "8 bit control word").

15. As for **Claims 11, 22, 36, and 47**, Johnson et al. disclose wherein the digital input signal contains a plurality of bits (see paragraph 0067, lines 20 – 22, "8 bit control word").

16. As for **Claims 12, 23, 37, and 48**, Johnson et al. disclose, as shown in figure 11, wherein a first portion of the bits is applied to the CDS (CDSVAGA 114) to set the gain of the CDS and a second portion of the bits is applied to the PGA (digital gain 117) to set the gain in the PGA (see paragraphs 0073).

17. As for **Claims 13, 24, 38, and 49**, Johnson et al. disclose wherein an overall gain of the system comprises a combination of gain in the CDS and gain in the PGA (see paragraphs 0071 and 0072).

18. As for **Claims 21 and 46**, Johnson et al. disclose wherein gain in the CDS is settable by a digital input signal (see paragraph 0067, lines 20 – 22, "8 bit control word") and wherein gain of the PGA is settable by a digital input signal (see paragraph 0067, lines 20 – 22, "8 bit control word").

19. As for **Claims 14, 25, 39, and 50**, Johnson et al. disclose, as stated in paragraphs 0071 and 0072, wherein the overall gain is pseudo-logarithmic.

Claim Rejections - 35 USC § 103

20. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

21. **Claims 3, 17, 28, and 42** are rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson et al. (US 2002/0176009) in view of Lee et al. (US 6,388,500 B1).

22. As for **Claims 3, 17, 28, and 42**, Johnson et al. disclose a correlated double sampler (CDSVGA 114) for receiving the input signal (VIN) comprising an amplifier for amplifying the input signal (see figure 5) and a programmable gain amplifier (digital gain 117; see figure 8) for receiving the output signal from the CDS (CDSVGA 114) and amplifying the received signal (see figure 3, the output of the CDSVAGA 114 is passed through ADC 116 and on to digital gain 117).

However, Johnson et al. do not specifically disclose wherein the gain in the CDS is settable to one of four levels.

On the other hand, Lee et al. also teach an image processing system with a CDS and programmable gain amplifier. More specifically, Lee et al. teach, as shown in 4, an image processing system (80) with a CDS (82) and programmable gain amplifier (84) that is part of the CDS. Furthermore, Lee et al. teach wherein gain in the CDS is at least settable to four levels (see column 5, lines 39 – 45). Therefore, Lee et al. teach wherein the gain in the CDS is settable to one of four levels.

At the time the invention was made, it would have been obvious to one with ordinary skill in the art to have provided wherein the gain in the CDS is settable to one of four levels, as taught by Lee et al., in the image processing system with a CDS and programmable gain amplifier, disclosed by Johnson et al., for the advantage of very quickly controlling the gain of an input signal with low power consumption (see Lee et al., column 3, lines 11 - 15).

Conclusion

23. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

24. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Justin P Misleh whose telephone number is 571.272.7313. The Examiner can normally be reached on Monday through Friday from 8:00 AM to 5:00 PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Lin Ye can be reached on 571.272.7372. The fax phone number for the organization where this application or proceeding is assigned is 571.273.8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Justin Misleh
Examiner, GAU 2622
November 10, 2007

LIN YE
SUPERVISORY PATENT EXAMINER

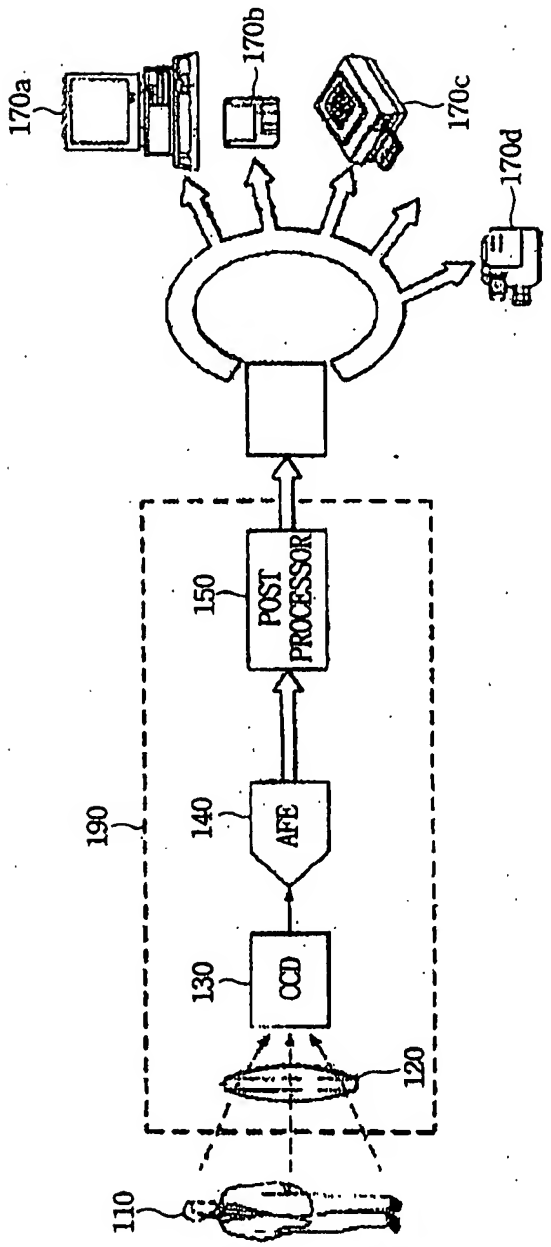

FIG. 1
(PRIOR ART)

PLEASE ENTER 11/9/07

FIG. 2
(PRIOR ART)

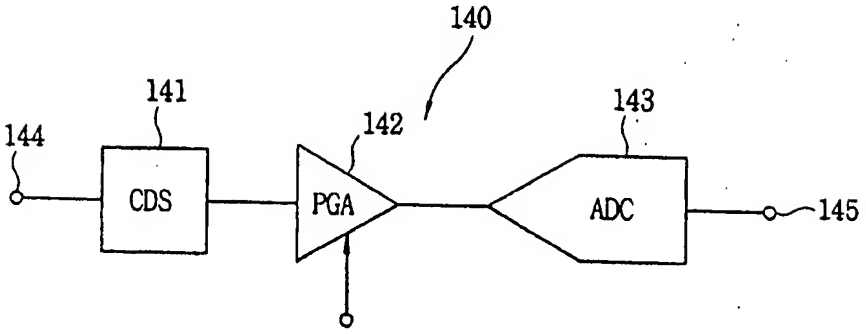

FIG. 3
(PRIOR ART)